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10/813,615	03/31/2004	Simon Knowles	66365-020	3818

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EXAMINER	
FIEGLE, RYAN PAUL	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,615	KNOWLES, SIMON	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 19 and 21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. "Program code means" could include written code.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. The terms "relatively narrower" and "relatively wider" in claims 1 and 18 are relative terms which renders the claims indefinite. The terms "relatively narrower" and "relatively wider" are not defined by the claims, the specification does not provide a

standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. There is no way to determine what these widths are "relative" to.

7. Claim 20 recites the limitation "the two instructions selected" in 17. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 2, 7, 11, 14-16 and 18-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Kahle et al. (USPGPub 2005/0044434).

10. As per claim 1:

A computer processor, the processor comprising:

a decode unit for decoding instruction packets fetched from a memory holding a sequence of instruction packets (¶0016); and

first and second processing channels, each channel comprising a plurality of functional units, wherein the first processing channel is capable of performing control operations and comprises a control register file having a relatively narrower bit width

(¶0016; Figure 1, item 26), and the second processing channel is capable of performing data processing operations at least one input of which is a vector and comprises a data register file having a relatively wider bit width (¶0016; Figure 1, items 20, 28, 30, 32 and 34);

wherein the decode unit is operable to detect for each instruction packet whether the instruction packet defines (i) a plurality of control instructions to be executed sequentially on the first processing channel or (ii) a plurality of instructions comprising at least one data processing instruction to be executed simultaneously on the second execution channel, and to control the first and second channels in dependence on said detection (It is inherent that instructions are issued to the proper functional unit based on opcode).

11. As per claim 2:

A computer processor according to claim 1, wherein the first processing channel further comprises a branch unit and a control execution unit (¶0016).

12. As per claim 7:

A computer processor according to claim 1, wherein the instruction packets are all of equal bit length.

Kahle was made for use with the PowerPC architecture as noted by the use of the VMX unit and mention of the architecture (¶0005). PowerPC fetches exactly eight instructions every cycle.

13. As per claim 11:

A computer processor according to claim 7, wherein the nature of each instruction in an instruction packet is selected at least from a control instruction, a data instruction, and a memory access instruction (¶0016).

14. As per claim 14:

A computer processor according to claim 1, wherein when the decode unit detects that the instruction packet defines three control instructions, the decode unit is operable to supply the first processing channel with the three control instructions whereby the three control instructions are executed sequentially.

PowerPC dispatches 5 instructions at a time in sequential order. In the occurrence of three control instructions being present in this group, the decode unit (issue unit) will dispatch the instructions to the control unit (Figure 1, item 26).

15. As per claim 15:

A computer processor according to claim 1, wherein when the decode unit detects that the instruction packet defines two instructions comprising at least one data instruction, the decode unit is operable to supply the second processing channel with at least the data instruction whereby the two instructions are executed simultaneously.

PowerPC dispatches 5 instructions at a time in sequential order. In the occurrence of two VMX instructions being present in this group, the decode unit (issue unit) will dispatch the instructions to the VMX unit (Figure 1, items 20, 28, 30, 32 and 34).

16. As per claim 16:

A computer processor according to claim 1, wherein the decode unit is operable to read the values of a set of designated bits at predetermined bit locations in each instruction packet of the sequence (Based on the definition of an instruction set architecture, it is inherent that the decode unit will read bits in predetermined bit locations in the instruction packet; the decoder has to determine what instructions are in the packet, this is done by reading the opcodes.), to determine:

a) whether the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction (In reading the opcodes the decoder will determine whether the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction); and

b) where the instruction packet defines a plurality of instructions of which at least one is a data instruction, the nature of each of the two instructions selected from: a control instruction; a data instruction; and a memory access instruction (¶0016).

17. As per claim 18:

A method of operating a computer processor which comprises first and second processing channels each comprising a plurality of functional units, wherein the first processing channel comprises a control register file having a relatively narrower bit width and the second processing channel comprises a data register file having a relatively wider bit width (¶0016), the method comprising:

decoding an instruction packet to detect whether the instruction packet defines a plurality of control instructions of equal length or two instructions comprising at least one data instruction, at least one of which is a vector (In reading the opcodes the decoder

will determine whether the instruction packet defines a plurality of control instructions of equal length or two instructions comprising at least one data instruction, at least one of which is a vector);

when the instruction packet defines a plurality of control instructions of equal length, supplying the control instructions to the first processing channel whereby the control instructions are executed sequentially (PowerPC dispatches 5 instructions at a time in sequential order. In the occurrence control instructions being present in this group, the decode unit (issue unit) will dispatch the instructions to the control unit (Figure 1, item 26)); and

when the instruction packet defines a plurality of instructions comprising at least one data instruction, supplying at least the data instruction to the second processing channel whereby the plurality of instructions are executed simultaneously (PowerPC dispatches 5 instructions at a time in sequential order. In the occurrence of VMX instructions being present in this group, the decode unit (issue unit) will dispatch the instructions to the VMX unit (Figure 1, items 20, 28, 30, 32 and 34)).

18. As per claim 19:

A computer program product comprising program code means which include a sequence of instruction packets,

said instruction packets including a first type of instruction packet comprising a plurality of control instructions of equal length and a second type of instruction packet comprising a plurality of instructions including at least one data instruction (PowerPC

does not place limitations on the contents of its packets. These scenarios are covered by the architecture.),

wherein the computer program product is adapted to run on a computer such that the first type of instruction packet is executed by a dedicated control processing channel, and the at least one data instruction of the second instruction packet is executed by a dedicated data processing channel, the dedicated control processing channel having a relatively narrower bit width than the dedicated data processing channel (¶0016).

While Kahle does not explicitly disclose a computer program product, such is inherent since the processor is useless without having program code to run on it.

19. As per claim 20:

A method of operating a computer processor which comprises first and second processing channels each comprising a plurality of functional units, wherein the first processing channel comprises a control register file having a relatively narrower bit width and the second processing channel comprises a data register file having a relatively wider bit width (¶0016), the method comprising:

fetching a sequence of instruction packets from a program memory, all of said instruction packets containing a set of designated bits at predetermined bit locations sequence (Based on the definition of an instruction set architecture, it is inherent that the decode unit will read bits in predetermined bit locations in the instruction packet; the decoder has to determine what instructions are in the packet, this is done by reading the opcodes.);

decoding each instruction packet, said decoding step including reading the values of said designated bits to determine:

a) whether the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction (In reading the opcodes the decoder will determine whether the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction); and

b) where the instruction packet defines a plurality of instructions of which at least one is a data instruction, the nature of each of the two instructions selected from: a control instruction; a data instruction; and a memory access instruction (¶0016).

20. As per claim 21:

A computer program product comprising program code means which include a sequence of instruction packets,

said instruction packets including a first type of instruction packet comprising a plurality of control instructions of substantially equal length and a second type of instruction packet comprising first and second instructions including at least one data instruction (PowerPC does not place limitations on the contents of its packets. These scenarios are covered by the architecture.),

said instruction packets including at least one indicator bit at a designated bit location within the instruction packet, wherein the computer program product is adapted to run on a computer such that said indication bit is adapted to cooperate with a decode unit of the computer to designate whether (Based on the definition of an instruction set architecture, it is inherent that the decode unit will read bits in predetermined bit

locations in the instruction packet; the decoder has to determine what instructions are in the packet, this is done by reading the opcodes.):

a) the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction (In reading the opcodes the decoder will determine whether the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction); and

b) in the case when there is a plurality of instructions comprising at least one data instruction, the nature of each of the two instructions selected from: a control instruction; a data instruction; and a memory access instruction (¶0016).

While Kahle does not explicitly disclose a computer program product, such is inherent since the processor is useless without having program code to run on it.

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 3, 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle et al. (USPGPub 2005/0044434) as applied to claim 1 above in view of "Unifying FPGAs and SIMD Arrays" by Bolotski et al.

23. As per claim 3:

Kahle teaches the computer processor according to claim 1, wherein the second processing channel further comprises a fixed data execution unit (Kahle: ¶0016).

Kahle does not disclose the second processing channel containing a configurable data execution unit.

Bolotski teaches a system that can simulate SIMD and configurable operations on the same unit, which can be subdivided into SIMD, and configurable units (Bolotski: §4).

Bolotski comments on the benefits of combining a SIMD and configurable unit, including reducing cost by not duplicating logic (Bolotski: §4.1).

The advantages of configurable units are well known in the art (Bolotski: §1).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art to apply a configurable unit to Kahle by modifying the VMX as in Bolotski to do the tasks of SIMD operations as well as configurable operations.

24. As per claim 4:

A computer processor according to claim 3, wherein the fixed data execution unit and the configurable data execution unit both operate according to a single instruction multiple data format (Bolotski: §4).

25. As per claim 17:

A computer processor according to claim 3, wherein the configurable data execution unit is capable of executing more than two consecutive operations on the data provided by a single issued instruction before returning a result to a destination register file.

One of ordinary skill in the pertinent art would have recognized that this is a simple accumulate function that would be easily programmable in configurable logic.

26. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle et al. (USPGPub 2005/0044434) as applied to claim 1 above in view of Fuller (US Patent 5,423,051).

27. As per claim 5:

Kahle does not teach the computer processor according to claim 1, wherein the first and second processing channels share a load store unit while Fuller does (Fuller: Figure 6).

Such would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention since sharing hardware precludes the need to duplicate it, which saves power and die space.

28. As per claim 6:

A computer processor according to claim 5, wherein the load store unit uses control information supplied by the first processing channel and data supplied by the second processing channel (Fuller: Figure 6).

29. Claims 8-10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kahle et al. (USPGPub 2005/0044434) as applied to claim 1 above.

30. These claims recite limitations of the bit lengths of various instructions and packets.

While Kahle may not teach the recited lengths, such modifications would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's

invention. Making a bit length longer or shorter is done for multiple reasons well known in the art. For example, Kahle points out the advantages of longer bit lengths, including increased precision (Kahle: ¶0006). Further, shortening a bit length has known advantages, such as saving storage space and reducing complexity of logic.

If it was advantageous to lengthen or shorten the bit lengths in Kahle for various reasons, one of ordinary skill in the pertinent art would have recognized that it would have been simple to do so.

Further, it has been found that a change in size does not produce a patentable distinction. In re Rose , 220 F.2d 459, 105 USPQ 237 (CCPA 1955) (Claims directed to a lumber package "of appreciable size and weight requiring handling by a lift truck" where held unpatentable over prior art lumber packages which could be lifted by hand because limitations relating to the size of the package were not sufficient to patentably distinguish over the prior art.); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976) ("mere scaling up of a prior art process capable of being scaled up, if such were the case, would not establish patentability in a claim to an old process so scaled." 531 F.2d at 1053, 189 USPQ at 148.).

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"A Brief Look at the PowerPC 970" by Stokes gives a simple, comprehensible synopsis of the fetching, decoding, and issuing within the PowerPC architecture. A

plain text version is being transmitted with this correspondence. The original article can be viewed at: http://arstechnica.com/wankerdesk/3q02/powerpc.html

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan P Fiegle
Examiner
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